MBI5051/MBI5052/MBI5053 Application Note

Forward

MBI5051/52/53 uses the embedded Pulse Width Modulation (PWM) to control LED current. In contrast to the traditional LED driver uses an external PWM signal to achieve the PWM function, MBI5051/52/53 has more outstanding behavior in gray scale performance and is suitable for LED full-color display.

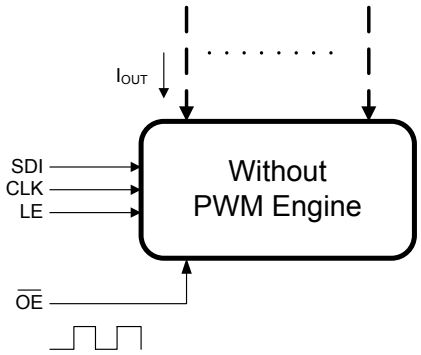

Figure 1. The traditional LED driver

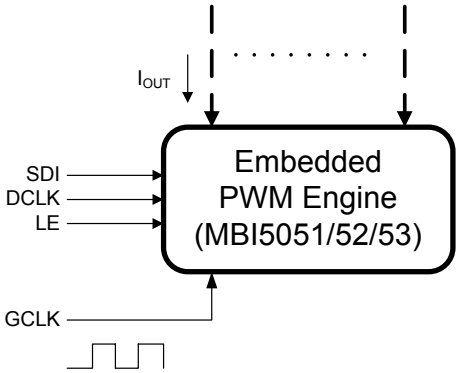

Figure 2. PWM-Embedded LED driver

Figure 1 shows the scheme of the traditional LED driver. It controls the LED current (I_{OUT}) and brightness by PWM signal through $\overline{OE}$ pin. The signal of $\overline{OE}$ will suffer distortion and decay in long distance transmission, and furthermore causing poor LED brightness control while using more gray scale bits. Figure 2 is the scheme of PWM-Embedded LED driver, the Gray Scale Clock (GCLK) is used to trigger the internal PWM counter and output a PWM pulse to control the LED current. Even in the applications of long distance transmission and high gray scale bits, the distorted and decayed GCLK will not affect the LED brightness control. Since GCLK is the trigger of PWM counter, the variable pulse width won't affect the internal PWM.

Moreover, the traditional PWM-Embedded LED driver requires a very fast DCLK frequency to input new data when the scan line changed. However, by MBI5051/52/53, the whole frame data can be inputted due to the embedded 4/8/16 bit SRAM, therefore the DCLK frequency can be slower. Compare to the traditional PWM driver, the MBI5051/52/53 can achieve higher gray scale in time multiplexing application.

This article provides the application information of MBI5051/52/53, such as the input method of image data and the setting of gray scale data. The detail operations are described in the following section.

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Section 1: Principle of Operations

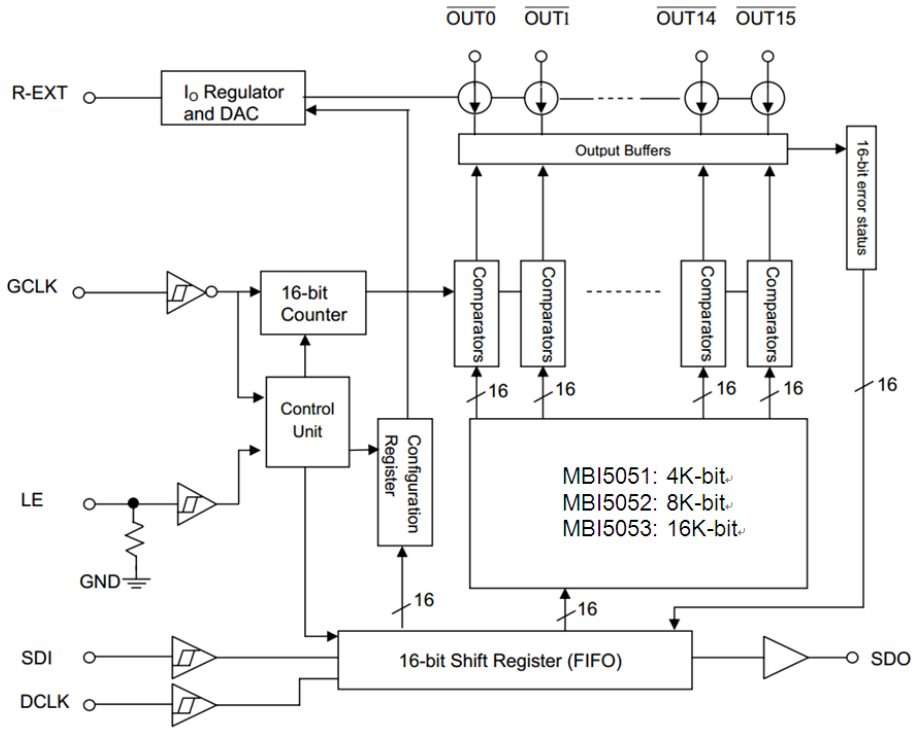

Figure 3. Internal block diagram of MBI5051/52/53

Figure 3 shows the internal block diagram of MBI5051/52/53, the function of each pin is described below.

Input Pins of Control Signals

DCLK: Data Clock Input pin

SDI: Gray Scale Data Input pin

LE: The combination of LE and DCLK can be used to control command.

The gray scale data of MBI5051/52/53 is the combination of DCLK, SDI and LE. On the rising edge of DCLK, MBI5051/52/53 reads one bit data from SDI pin and inputs to the internal 16-bit shift register. The LE pin handles the “data latch” command of the internal 16-bit shift register.

Control Signals Output Pin

SDO: Serial Data Output pin. The SDO of first device is connected to the SDI pin of second device and so on. The gray scale data can be sent to next IC.

PWM Counter Clock Input Pin

GCLK: PWM Counter Input pin. The frequency of GCLK determines the count speed of the internal PWM counter, and also the output frequency of $\overline{OUT0}$~$\overline{OUT15}$.

Current Setting Pin

R-EXT: This pin is used to connect an external resistor to set up the output current for all output channels.

LED Driver Output Pin

$\overline{OUT0}$~$\overline{OUT15}$: Output Channel pins. Connects to the LED and controls the LED current.

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Section 2: The Basic Settings of Gray Scale

In the time multiplexing application, the sequence of input data starts from scan line 1, scan line 2, until scan line M (M≦8/16/32). MBI5051/52/53's 16 channels can perform different gray scale data individually, so the data length of 16 channels must be 256 bits (16 bits x 16 channels =256 bits).

Example 1

Number of IC: 1

Number of scan line: 32

Depth of PWM control: 16- bit

As shown in figure 4, the data of ch15 need to be sent first, and then follow the sequence of ch14to ch0, and then LE executes the data latch.

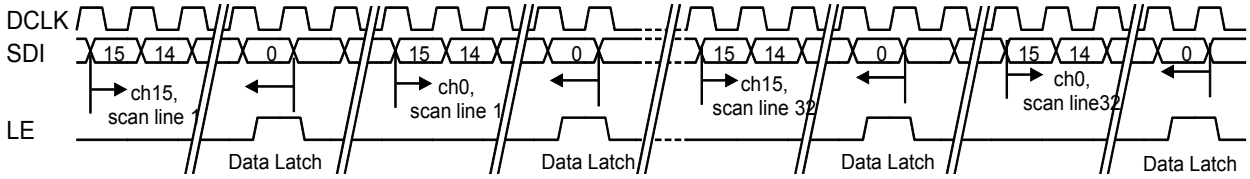

Figure 4. The timing diagram of 16-bit gray scale data

The 14- bit gray scale can be set through Bit [7]=1 in configuration register.

Example 2

Number of IC: 1

Number of scan lines: 32

Depth of PWM control: 14- bit

As shown in Figure 5, the data format is same as 16-bit gray scale data, only the last 2-bit (LSB) is "0".

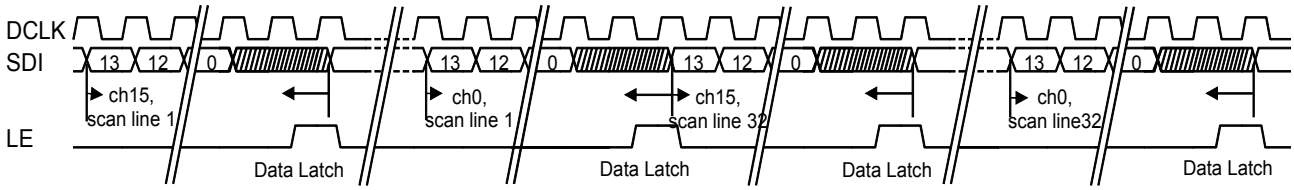

Figure 5. The timing diagram of 14-bit gray scale data

The gray scale data needs the GCLK to save the data into SRAM. The frequency of GCLK must be higher than 20% of DCLK to get the correct data.

After the last data latch command, it needs at least 50 GCLKs to read the gray scale data into internal display buffer before the Vsync command comes. And display is updated immediately until MBI5051/52/53 receives the Vsync signal (high pulse of LE pin is sampled by 3-DCLK rising edges), as figure 6 shows.

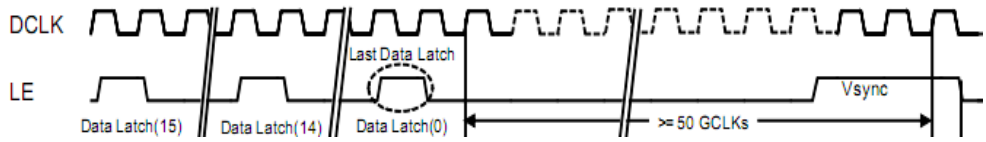

Figure 6. Vertical Sync

Section 3: The settings of gray scale data to the cascade of several MBI5051/52/53

If there are N pieces of MBI5051/52/53 in cascaded as Figure 7 shows, then the data length of each “data latch” will be 16 x N bits.

For one MBI5051/52/53, each latch needs 16-bits of grayscale data.

For two MBI5051/52/53 in cascaded, each latch needs 32-bits of grayscale data, and so on.

But no matter how many MBI5051/52/53 in cascaded, the latch signal only can be executed until all the data are ready, as figure 8 shows.

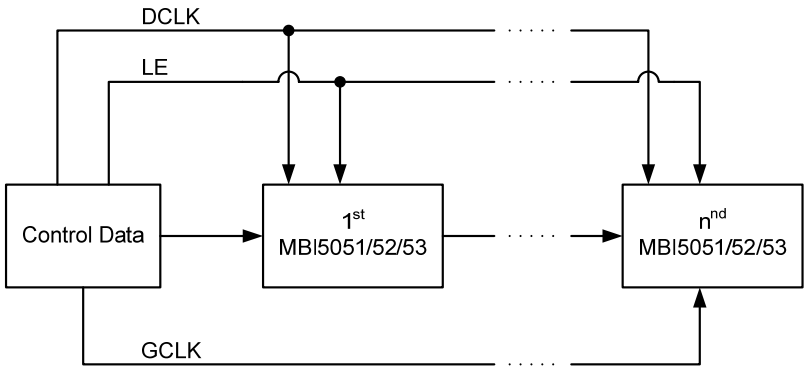

Figure 7. n pieces of MBI5051/52/53 in cascaded

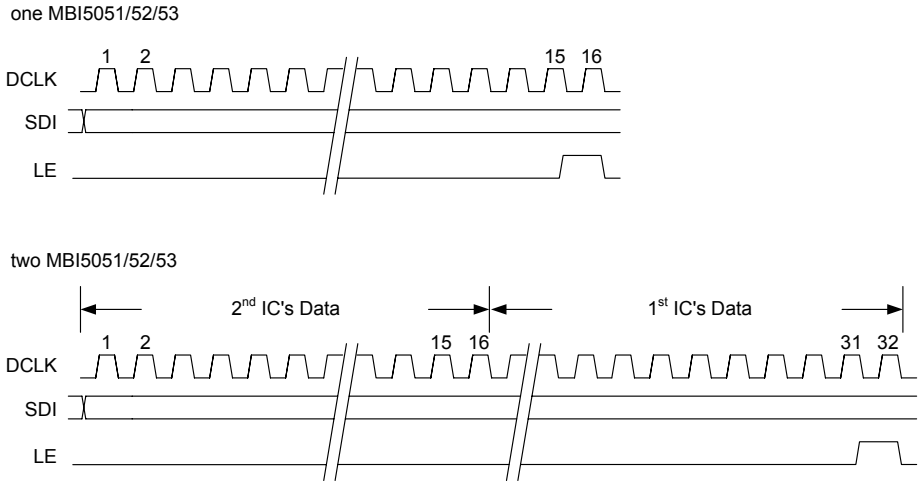

Figure 8. The timing diagram of “data latch” command

Section 4: Read/Write Configuration Register

MBI5051/52/53 embeds a readable and writeable configuration register which can determine the operation mode. The configuration register includes current gain adjustment, ghost-cancelling, and etc.

Figure 9 shows the control command of write configuration. Pre-Active command (high pulse of LE pin is sampled by 14-DCLK rising edges) must be executed before the write configuration command, and then the data can write into the configuration register. Each data length of MBI5051/52/53 is 16-bit, if there are N pieces of IC in cascaded, the 16xN bits date, which is forward counting from the LE falling edge, will be latched into the configuration register.

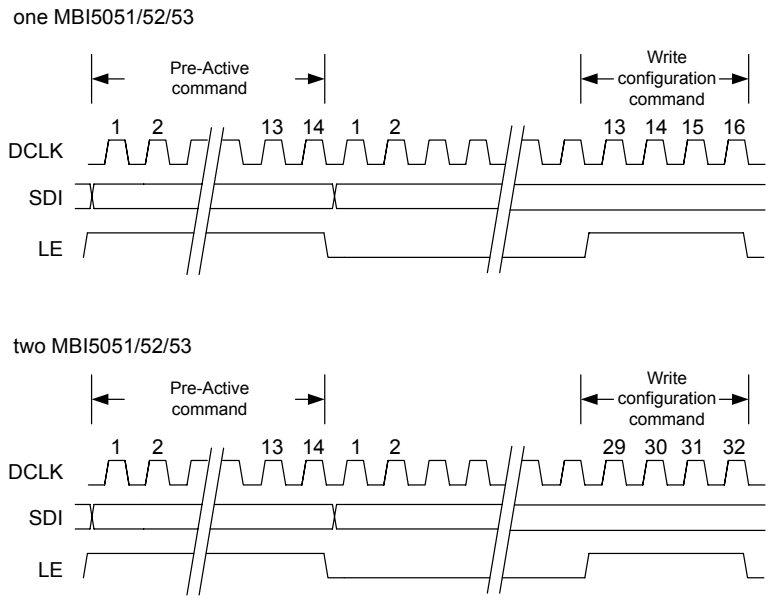

Figure 9. The waveform of writing data into configuration register

The data sequence starts from 2nd MBI501/52/53, and then the 1st IC. Each data starts from MSB. In the durations of Pre-Active command and Write Configuration command, LE must pull to low to prevent leaving the Pre-Active mode and the configuration data becomes invalid.

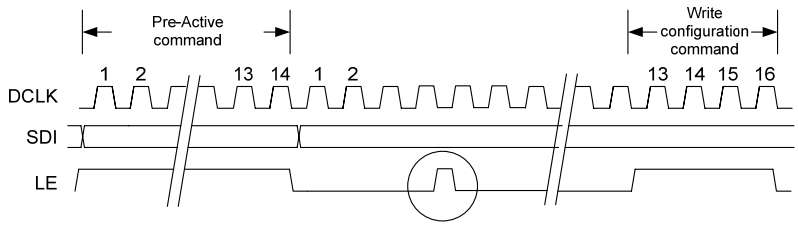

Figure 10. Example of incorrect LE signal - 1

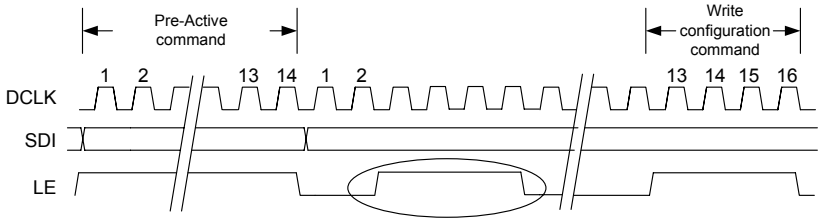

Figure 11. Example of incorrect LE signal - 2

Figure 13 shows the control command of Read Configuration. Any moment, once the LE high pulse is sampled by 5-DCLK rising edges, the first bit in configuration register will be outputted from SDO, and then each bit comes out with DCLK.

The sequence of read data starts from 2nd MBI5051/52/53, and then the 1st IC. In the duration of Read Configuration, the SDI signal can be ignored.

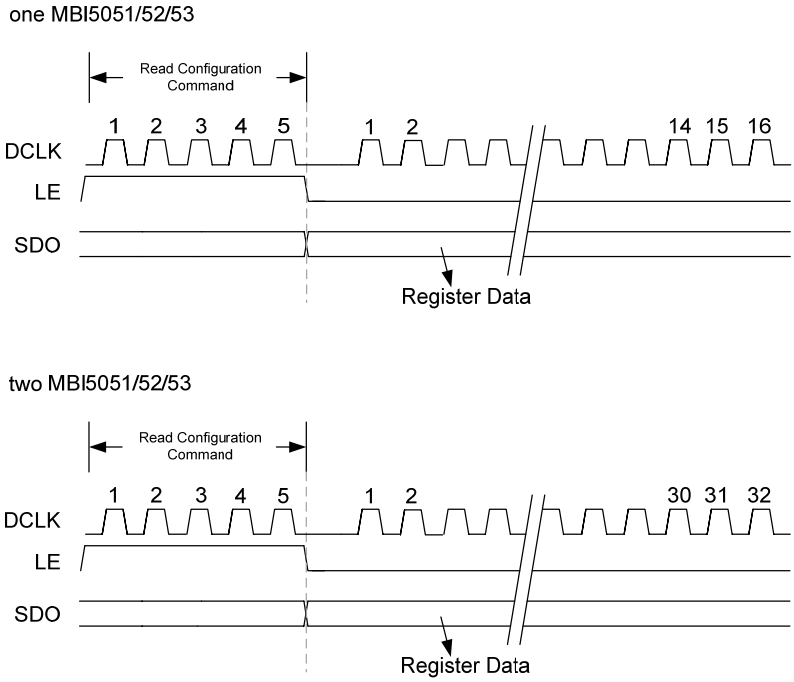

Figure 12. The diagram of reading data from configuration register

Section 5: Send Data and Display Image

MBI5051/52/53 embeds 4/8/16k-bit SRAM and divides it into two banks to reading and writing data frame. As figure 13 shows, the gray scale data of next frame can be sent while current frame is playing. After receive the Vsync command, the SRAM will switch the function of these two banks to reading and writing.

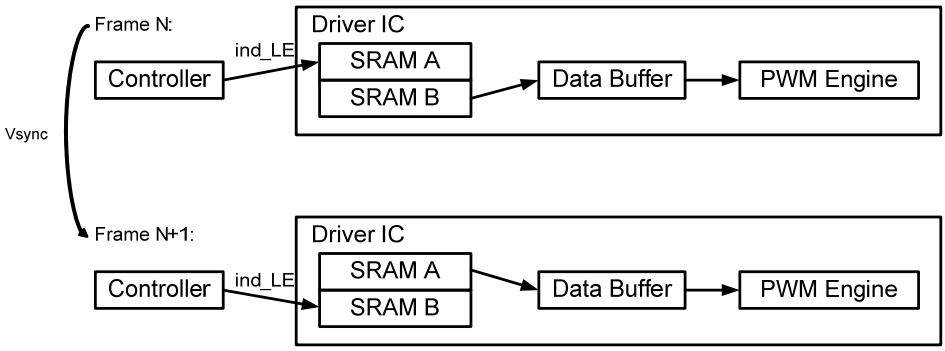

Figure 13. The data transmission structure of MBI5051/52/53

Section 6. Visual Refresh Rate and GCLK Multiplier Technology

With Scrambled-PWM (S-PWM) technology, MBI5051/52/53 enhances pulse width modulation by scrambling the “on” time into several small “on” periods. Thus the technology increases the visual refresh rate. The data refresh rate and pulse width in different image data can be calculated from the following formals.

Visual Refresh Rate

With Scrambled-PWM technology, the 65536 GCLKs (16-bits) PWM cycle of MBI5051/52/53 is divided into 64 sections, each section has 1024 GCLKs. The 16384 GCLKs (14-bit) PWM cycle of MBI5051 is divided into 16 sections, each section has 1024 GCLKs. The 16384 GCLKs (14-bit) PWM cycle of MBI5052/53 is divided into 32 sections, each section has 512 GCLKs.

The formulas of visual refresh rate are

In 16-bit S-PWM mode, visual refresh rate $F_{visual} = F_{GCLK} / [(1024 + t_{Dead}) \times N]$ ..... (1)

In 14-bit S-PWM mode, visual refresh rate $F_{visual} = F_{GCLK} / [(512 + t_{Dead}) \times N]$ ..... (2)

where

F_{visual}: Visual Refresh Rate.

F_{GCLK}: Gray Scale Clock Frequency.

t_{Dead}: Dead Time.

N: Number of Scan Lines.

For example, in the 32:1 time multiplexing application, whose driver is MBI5053, a 16-bit SPWM driver, the GCLK frequency is 15MHz, then the visual refresh rate could be calculated as below

F_{visual} =15MHz/[(1024+10)x32]=453

The MBI5051/52/53 provides a SRAM to save the frame data, the updated data transmission has to be completed before next frame. The GCLK frequency needn't to follow the frame rate.

For example, if MBI5053's GCLK is 15MHz, the dead time is 10 GCLK. The cycle number of GCLK=15MHz in a period is shown as table 1.

Table 1. The cycle numbers of GCLK=15MHz in a period

Case	Bit numbers of gray scale control(bit)	Frame rate (Hz)	Duty cycle of multiplexing design	Cycle number of GCLK counter in a period T_{DATA}
1	16	60	1/32 duty	7
2	16	50	1/16 duty	18
3	14	60	1/32 duty	14
4	14	50	1/16 duty	35

If the driver with 16-bit gray scale data, it needs 64 cycle number to complete a frame data. That means both case 1 and 2 don't have enough time to complete a frame data transmission. Increase the GCLK frequency of reduce the scan line is helpful to achieve this mission. Also, if the driver with 14-bit gray scale data, it needs 32 cycle number to complete a frame data. From above table, only case 4 can achieve this mission.

GCLK Multiplier Technology

If GCLK multiplier is enabled, GCLK will be dual edge triggered, that means the cycle time can be reduced by half. Table 2 shows the results of GCLK multiplier enabled.

Table 2. The cycle number of GCLK=15MHz when GCLK multiplier enabled

Case	Bit numbers of gray scale control(bit)	Frame rate (Hz)	Duty cycle of multiplexing design	Cycle number of GCLK counter in a period T_{DATA}
1	16	60	1/32 duty	15
2	16	50	1/16 duty	36
3	14	60	1/32 duty	29
4	14	50	1/16 duty	71

The Bits 15~7 are used to define the refresh rate (the SDI must larger than 64). The minimum output pulse width is the reciprocal of GCLK frequency.

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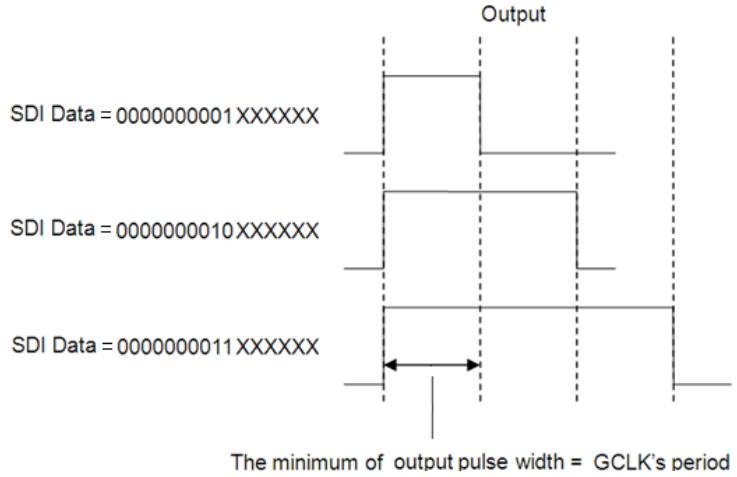

Figure 14. The diagram of SDI data and pulse width

Section 7: The Maximum Cascaded Number of MBI5051/52/53

The frame data must be updated in a picture period. Therefore, the maximum cascaded number of MBI5051/52/53 is decided by DCLK frequency and scan lines, and it can be calculated from the following equation

$$N = (F_{DCLK} \times duty) / (\text{the amount of data bit} \times \text{frame rate}) \quad \text{..... (3)}$$

For example, if the frame rate is 60 times/s, DCLK frequency is 15MHz, and duty is 1/16. Then from (3), the maximum cascaded number of MBI5051/52/53 is $N = [(15 \times 10^6) \times (1/16)]/(16 \times 16 \times 60) = 61$. Table 3 shows the maximum cascaded number of MBI5051/52/53 under different conditions.

Table 3. The maximum cascaded number of MBI5051/52/53 at DCLK=15MHz

Case	Frame rate (Hz)	Duty cycle of T_{DATA}	The maximum cascaded number of MBI5051/52/53
1	60	1/4 duty	244
2	60	1/8 duty	122
3	60	1/16 duty	61
4	60	1/32 duty	30
5	50	1/4 duty	292
6	50	1/8 duty	146
7	50	1/16 duty	73
8	50	1/32 duty	36

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Section 8: Current Gain

MBI5051/52/53 current gain can be adjusted from 12.5% (default) to 200%. No matter the output current is set by Rext or current gain, it should be controlled in the output current range of MBI5051/52/53; otherwise, the over designed output current can't be guaranteed.

The Bit 5 to Bit 0 in configuration register is used to set the current gain, and the defaulted gain code is 6'b101011. The Bit 5 is HC bit, HC=0 means in low current region, and HC=1 is high current region.

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Define	-	-	-	-	-	-					HC	DA4	DA3	DA2	DA1	DA0
Default	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1

6 bit gain code data

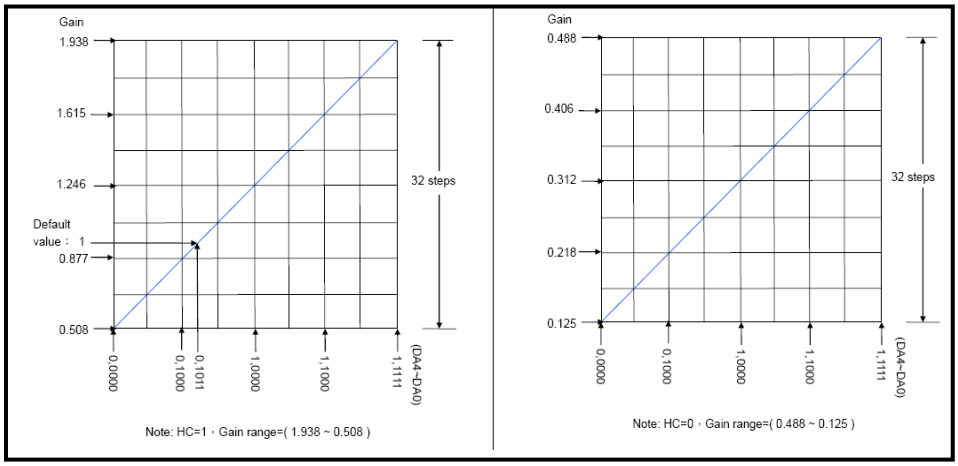

Figure 15. The relationship of current gain and gain code

The R_{ext} can be calculated by following equation

$$R_{ext} = (V_{R\text{-}EXT} / I_{OUT}) \times 23.0 \quad \text{..... (4)}$$

where $V_{R\text{-}EXT}$ = 0.61Volt ×G, and G means the current gain.

The relationship of current gain (G) and gain data (D) is

HC=1, D=(65xG-33)/3 ..... (5)

HC=0, D=(256xG-32)/3 ..... (6)

Example 1

If I_{OUT} =20mA and G=1, then the gain code is

Step 1: From (4), the R_{ext} = [(0.61 × 1) / 20mA] × 23 = 701.5Ω. From figure 15, G=1 in the high gain region, that means the HC=1. Thus, substitute above information into (5), the D=(65xG-33)/3=10.67≒11.

Step 2: Convert D into binary, D=01011, therefore DA[4:0]= 01011.

The 6 bits (bit 5~bit 0) of the configuration register are 6'b101011.

Example 2

If R_{ext} is 701.5Ω, the adjusted output current is from 20mA to 30mA, then

Step 1: G= 30mA /20mA =1.5 (HC=1).

Step 2: From (5), D= (65x1.5-33)/3=21.5≒ 22.

Step 3: Convert D into binary, D=01011, therefore DA[4:0]= 5'b10110.

Step 4: The adjusted gain code is 6'b110110.

Example 3

If R_{ext} is 701.5Ω, the adjusted output current is from 20mA to 5mA, then

Step 1: G= 5mA /20mA =0.25 (HC=0).

Step 2: From (6), D= (256x0.25-32)/3=10.67≒ 11.

Step 3: Convert D into binary, D=01011, therefore DA[4:0]= 5'b01011.

Step 4: The adjusted gain code is 6'b001011.

Figure 16 is the relationship of output current and gain data under V_{DD}=5.0V and R_{ext}=700Ω. The defaulted current gain, G =1, is corresponding to 20.6mA.

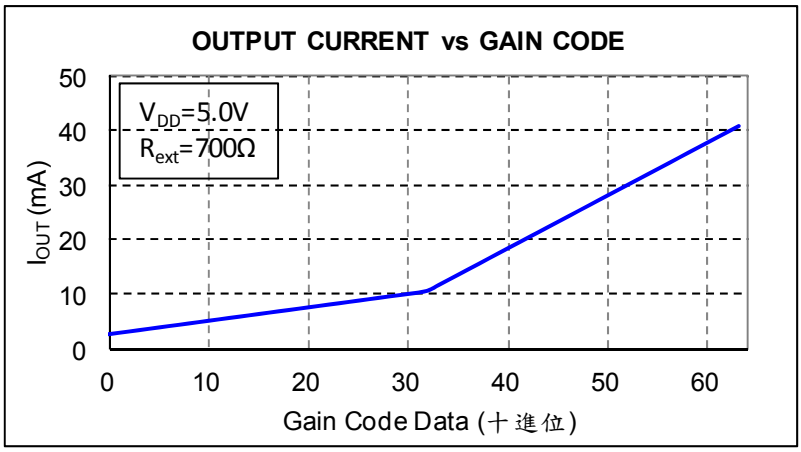

Figure 16. The relationship of current gain and code data under V_{DD}=5.0V and R_{ext}=700Ω.

Section 9: The Notice of LED Open-Circuit Detection

As figure 17 shows, MBI5051/52/53 executes the compulsory open-circuit detection while the LE high pulse is sampled by 7-DCLK rising edges. In the duration of compulsory open circuit detection, all the output channels will be turned off.

When LE high pulse pin is sampled by 1-DCLK rising edge, the result of open circuit detection will be shifted out from the SDO pin and the sequence is from MSB to LSB. The error detection will stop while the result is shifted out.

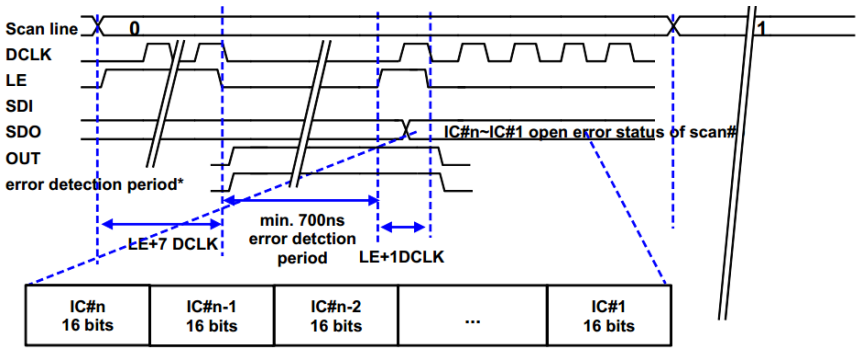

Figure 17. The timing waveform of compulsory error detection

In addition, please note the following items

1. In the duration of compulsory open circuit detection, the SDI data can be ignored until LE pin is sampled by 1-DCLK rising edge. The duration should be keep longer than 700ns, as figure 17 shows.
2. When output turns on, please make sure the output voltage (V_{DS}) is higher than 0.3V.
3. In the duration of compulsory open circuit detection, the scan line can't switch.
4. MBI5051/52/53 doesn't support LED short circuit deletion.
5. MBI5051/52/53 detects the LED open circuit once a scan line, however the detection result only can report which channel's LED is failed, can't exactly point out the failed LED in which scan line, this mission can be taken by controller.

Detected Result	Status
0	Open
1	Normal

Section 10: The Control Signal of Time Mulitplexing

Figure 18 shows an example of 4pcs MBI5053 in 32:1 time multiplexing application.

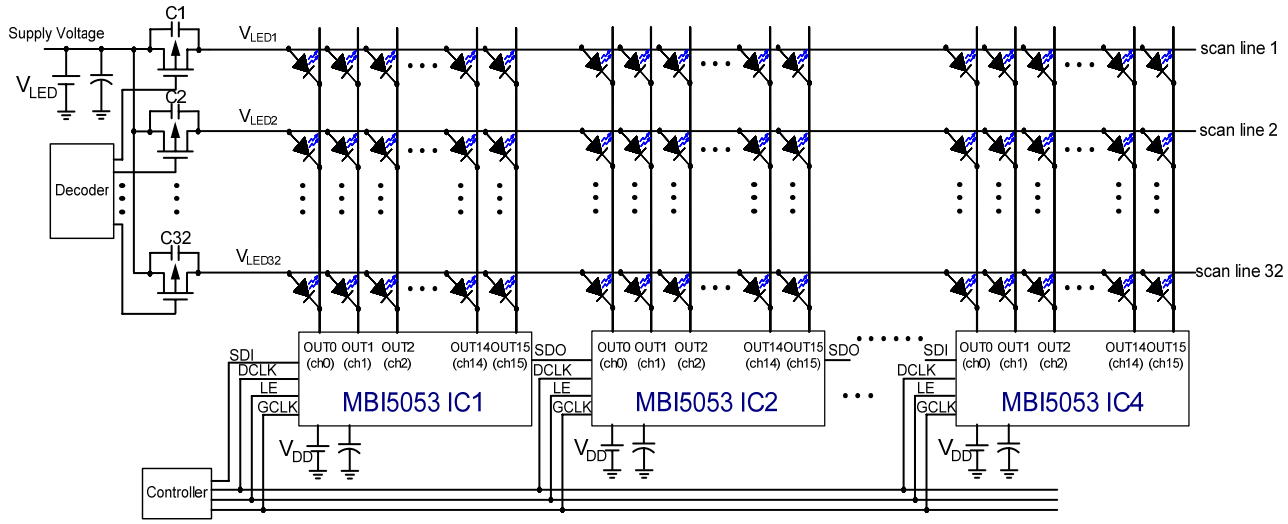

Figure 18. The schematic of time multiplexing application

In this example, the gray scale data is 2048 bits (4x16x32), and needs 512 times data latch (16x32).The Vsync command, which is used to update the frame data, should be executed at least 50 GCLK later than the last data latch. In the duration of Vsync command, the GCLK should be stopped.

Step 1. The Sequence of Gray Scale Data

Figure 19 shows the sequence of gray scale data. The bit63~bit48 are the gray scale data of 4th IC's /OUT15, and bit15~bit0 are the 1st IC's. A data latch command puts these data into SRAM buffer and then continue the data input of next output channel. After finish the data input of 1st scan line, then repeat above sequence to complete the others scan line's data.

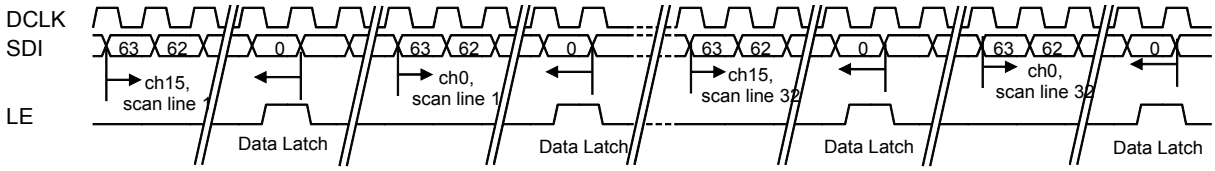

Figure 19. The sequence of gray scale data

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Step 2. The Frame Data Update Command, Vsync GCLK≠DCLK

The Vsync command should be executed at least 50-GCLK later than the last data latch, the reason of this spent time is to read the gray scale data from SRAM. Figure 20 shows the limitations of Vsync command, and followings are the further explain.

a.) The GCLK should be stopped before the Vsync command. The hold and setup times must respectively meet the specifications of t_{SU2} and t_{H2} in datasheet.

b.) Dead time is the interval between each scan line, and it terminates when GCLK is acted. Since the frame data will be updated after Vsync command executed, the scan line should be switched from line 32 to line 1 to restart the new frame data.

c.) In the duration of dead time, the DCLK must be stopped, and don't execute the data latch command.

d.) In the duration of dead time, the new data will be loaded in the internal display buffer, and the data will be showed on after the dead time.

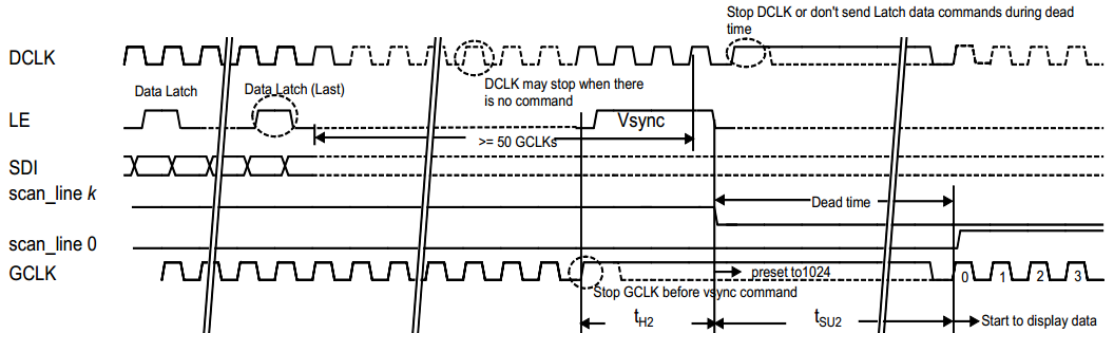

Figure 20. The timing waveform of Vsync (GCLK≠DCLK)

GCLK = DCLK

The differences from GCLK≠DCLK are

a.) Due to the GCLK=DCLK, the DCLK can't stop even the frame data and command have completed transmission.

b.) The DCLK has to stop after executed the Vsync command. The hold and setup times must respectively meet the specifications of t_{SU2} and t_{H2} in datasheet

c.) The DCLK must stop before the GCLK counter is 1023.

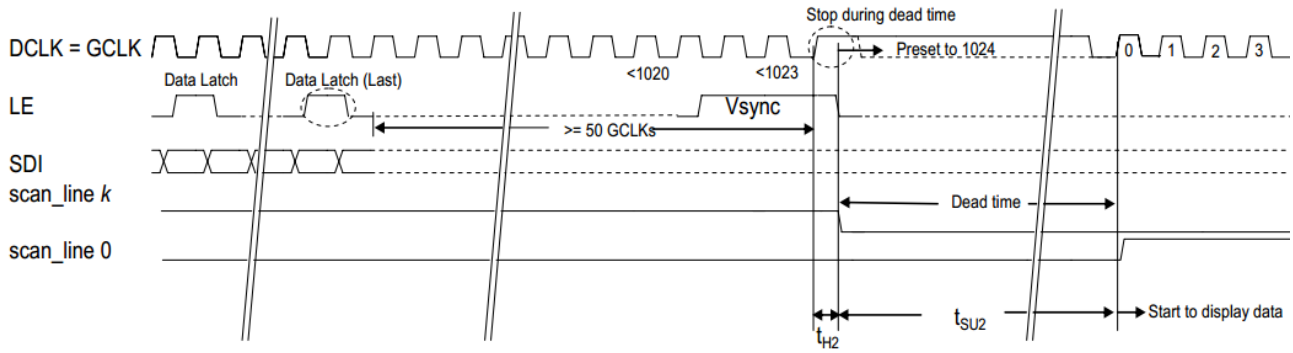

Figure 21. The timing waveform of Vsync (GCLK=DCLK)

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Step 3. Scan Line Switching

The gray scale data of MBI5051/52/53 are stored in the SRAM and use the technology of scrambled-PWM to improve the refresh rate. An extra GCLK is needed to switch the scan line when GCLK is counting from 0 to 1023. The dead time is determined by the duration of suspended GCLK. When the GCLK counter is 1024, all the output channels will be turned off in the dead time. Figure 22 shows the timing waveform.

Note: Once the amount of scan line is set in the status register, the amount of data string must same as the scan line to obtain normal display.

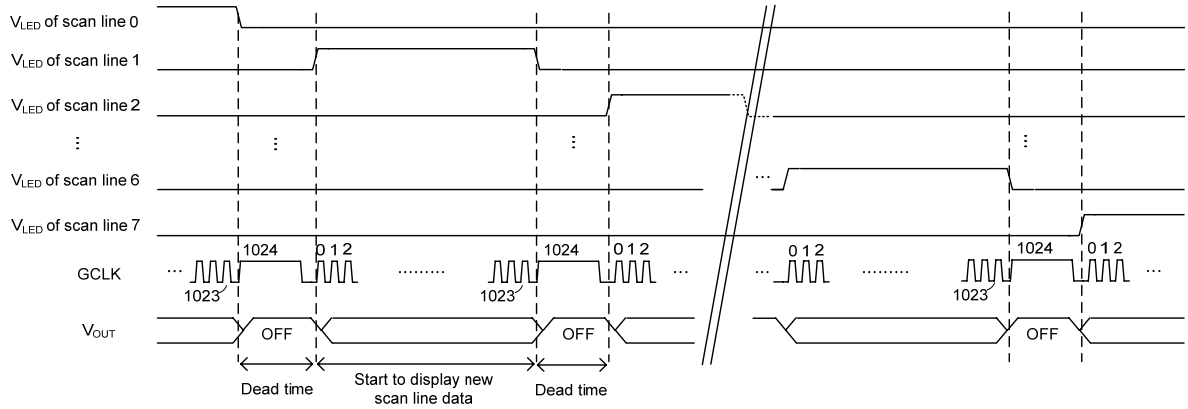

Figure 22. The timing waveform of switching scan line

Section 11. Ghost-Cancelling in the Time- Multiplexing LED Displays

The following actions can be taken to cancel the ghost effect in time multiplexing application.

Ghost-Cancelling

Figure 23 shows the diagram of the discharge/pre-charge circuit to cancel the ghost effect. The LEDs are turned on by the sequence of LED 0-0, LED 1-1⋯, LED n-15.

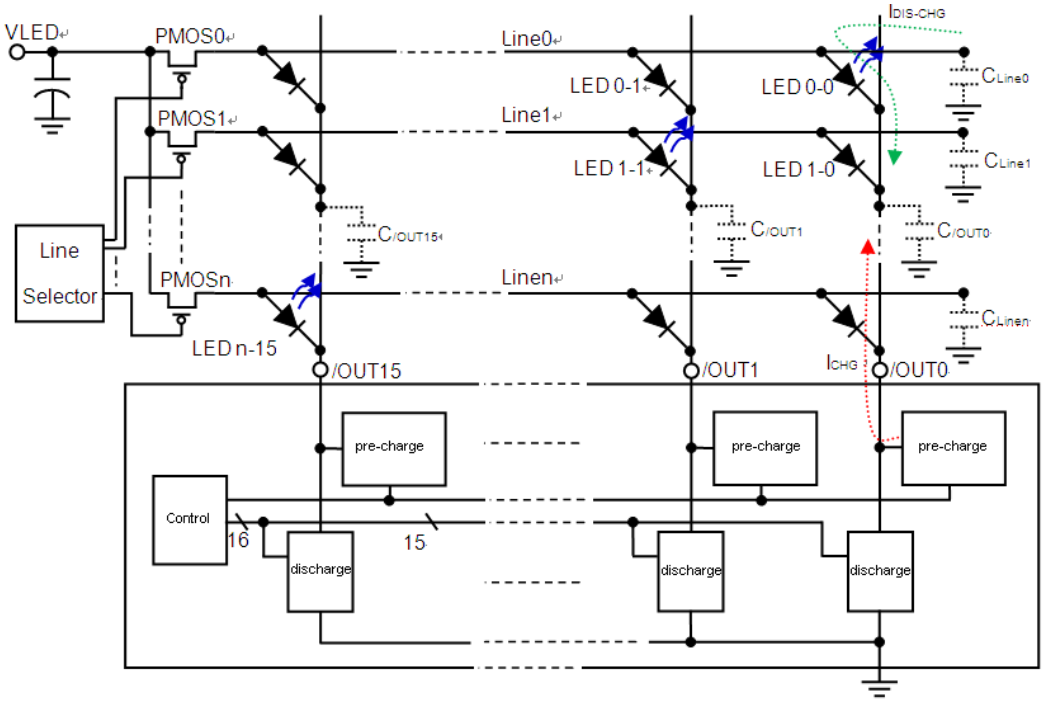

Figure 23. The diagram of the discharge/pre-charge circuit to eliminate the ghost effect

Ghost-Cancelling

The integrated ghost-cancelling feature can relieve the ghosting effect in time multiplexing LED display. The Bits E and F in status register are used to enable the functions, and figure 25 shows the timing waveform. An additional GCLK has to be inserted to present the dead time. To keep all the PMOS off while switching the scan lines. The high level of the additional GCLK determines the period of upper ghost-cancelling, and the low level is for lower ghost-cancelling.

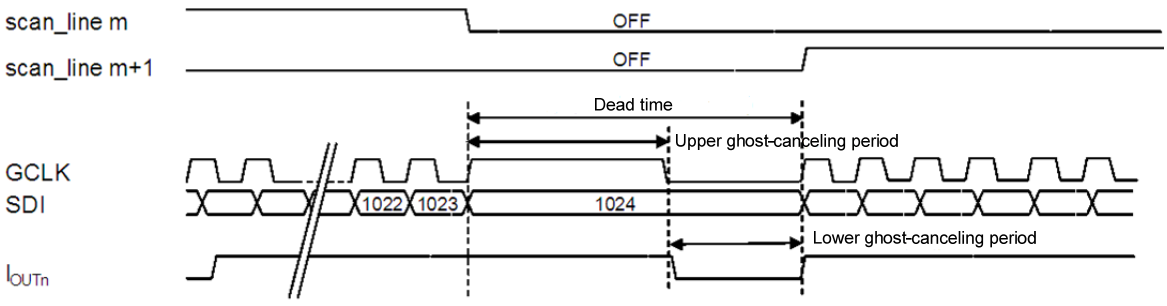

Figure 25. The timing waveform of upper and lower ghost-canceling

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When the ghost effect is happened in the time multiplexing LED display, enable both the Bit E and Bit F are recommended. Figure 26 is the display which hasn't enabled the ghost-cancelling function, and figure 27 is the enabled. In figure 27, the ghost effect has been complete cancel.

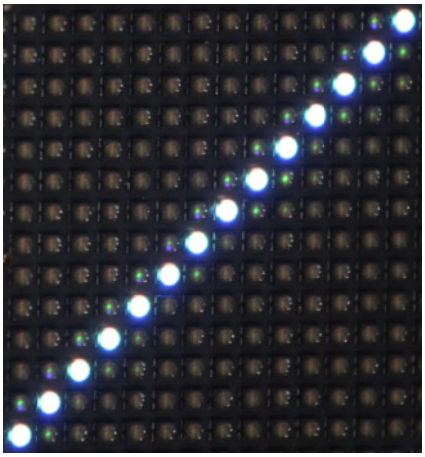

Figure 26. The display of disable upper/lower ghost cancelling

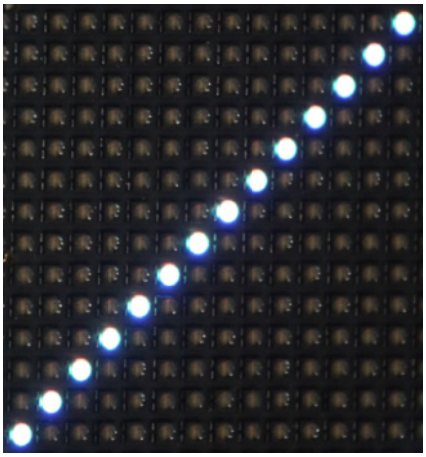

Figure 27. The display of enable upper/lower ghost cancelling

Section 12: Software Reset

When the software reset command is enabled, the internal counters of GCLK and data latch will be reset, and turned off all the output channels. However, the gray scale data stored in the SRAM, configuration register and current gain won't be reset.

Summary

MBI5051/52/53 uses the embedded S-PWM to control LED current and provides a storage solution of 4/8/16k-bit SRAM. Users don't need to send new data every time. This article provides the design guideline for uses.

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